Session 31 Overview

WLAN/Bluetooth

Chair: George Chien, *Marvell Semiconductor, Santa Clara, CA*

Associate Chair: Mototsugu Hamada, *Toshiba, Kawasaki, Japan*

The proliferation of wireless communication devices in recent years has driven their adoption into consumer electronics. The wide range of applications in the consumer markets demands lowest power (handheld devices), highest data rate (video distribution), highest level of integration (small form factor), and lowest cost (low component count). These requirements have been applied to the popular WLAN and Bluetooth devices in the previous years. In this session, a collection of current state-of-the-art devices that attempt to address each one of these requirements will be presented. These include an enhanced-data-rate (EDR) Bluetooth SoC that achieves Receiver/Transmitter (RX/TX) power of 38/48mW for low power, a multi-band MIMO transceiver IC that achieves >270Mb/s PHY rate for high throughput, an 802.11a/b/g SoC in 0.13µm CMOS, and an 802.11g SoC with integrated power amplifier implemented in 0.18µm CMOS for low cost.

In the area of low power consumption, Paper 31.1 from Broadcom describes a single-chip Bluetooth EDR device implemented in a 0.13µm CMOS technology. This transceiver integrates all the Bluetooth system building blocks, plus CPU, RAM/ROM and host interfaces. For low-voltage operation, an integrated low drop-out (LDO) voltage regulator is also included. This device achieves a low RX sensitivity of -84dBm for 3Mb/s while consuming only 38/48mW (in RX/TX mode) of power from a 1.5V supply.

In the high data rate area, the authors of Paper 31.2 from Broadcom and IQ Analog present a fully integrated multi-band MIMO transceiver for Draft-802.11n implemented in 0.18µm CMOS technology. This 2x2 MIMO transceiver integrates 2 complete transceivers on the same die with a single common LO. The paper addresses some of the key performance parameters for MIMO operation, such as I/Q imbalance, LO phase noise, and 40MHz operation. The measured phase noise at 100kHz offset is -108dBm/Hz while achieving the TX EVM of better than -40dB at -2dBm of output power. The paper concludes with a real-life demonstration of data throughput at the host interface level that reaches up to 200Mb/s while running at 270Mb/s PHY data rate.

For high integration, the authors of Paper 31.3 from Infineon and U Erlangen-Nuremburg describe an 802.11a/b/g SoC implemented in a 0.13µm CMOS technology. The RX achieves a sensitivity of -77/-74dBm for 2.4/5GHz bands and the TX outputs -2dBm with EVM better than -30dB. The die area for the RF transceiver is 6.7mm^2.

In the area of low component count/cost, the authors of Paper 31.4 from Atheros Communication and Stanford extend the integration level of an 802.11g SoC to include an RF front-end complete with a power amplifier (PA), low-noise amplifier (LNA), and a TX/RX switch all in a 0.18µm CMOS technology. This allows the possibility of connecting this SoC device directly to the antenna port to create a low-cost solution. The paper describes the circuit configuration that allows the sharing of RF ports between LNA and PA. The PA achieves +20dBm at 6Mb/s rate and an overall RX NF of 5.8dB.

31.1 A Single-Chip Bluetooth EDR Device in 0.13µm CMOS **1:30 PM**

B. Marholev, Broadcom, Irvine, CA

A low-power single-chip Bluetooth EDR device is realized using a configurable transformer-based RF front-end, a low-IF receiver and a direct-conversion transmitter architecture. It is implemented in a 0.13µm CMOS process and occupies 11.8mm^2. Sensitivity for 1, 2 and 3Mb/s rates is -88, -90, and -84dBm and transmitter differential EVM is 5.5% rms.

31.2 A Fully Integrated MIMO Multi-Band Direct-Conversion CMOS Transceiver for WLAN Applications (802.11n) **2:00 PM**

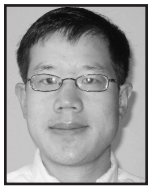
A. Behzad, Broadcom, San Diego, CA,

A single-chip multi-band direct-conversion CMOS MIMO transceiver (2×2) targeted for WLAN applications is presented. This transceiver is capable of satisfying the requirements of the Enhanced Wireless Consortium and achieves PHY rates of >270Mb/s. The receivers and transmitters achieve an EVM of better than -41dB (0.9%) and -40dB (1.0%) operating in legacy g and a modes, respectively. From a 1.8V supply and with both cores operating, the chip draws 275mA in RX mode and 280mA in TX mode.

31.3 An 802.11a/b/g RF Transceiver in an SoC **2:30 PM**

M. Simon, Infineon Technologies, Neubiberg, Germany

The RF transceiver of a 0.13µm CMOS WLAN 802.11a/b/g SoC for cellular applications comprising MAC, PHY, and analog front-end is presented. The transceiver with direct -conversion architecture and broadband 12GHz VCO draws 87/104mA in TX and 69/80mA in RX mode for the 2.4/5.0GHz band. The TX with control loop achieves -32dB EVM at -2dBm output power with 1.5V supply.



31.4 A Fully Integrated RF Front-End with Independent RX/TX Matching and +20dBm Output Power for WLAN Applications **3:15 PM**

R. Chang, Atheros Communications, Santa Clara, CA

An RF front-end for a WLAN SoC is implemented in 0.18µm CMOS. It integrates a +20dBm PA, a high-sensitivity LNA, and a T/R switch. The T/R switch incorporates an impedance-transformation network to provide a receive S_{11} of -15dB at 2.4GHz and a sensitivity of -73dBm for a 54Mb/s 802.11g signal. For 64QAM OFDM at 2.4GHz, the TX EVM is -25dB at an output power of +16dBm.